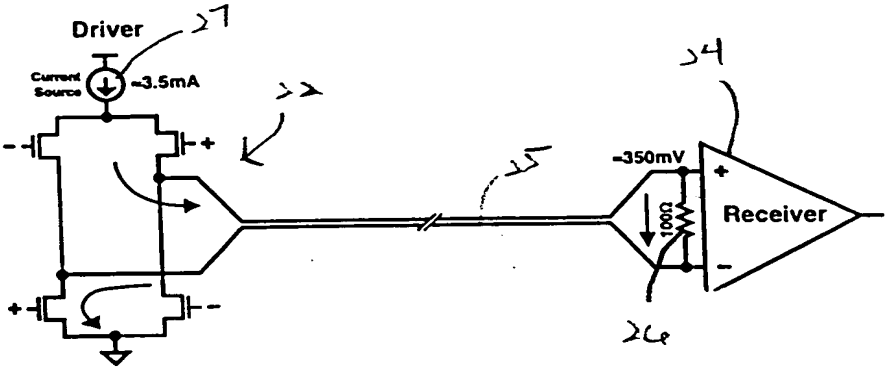

Fig. 1
(Prior Art)

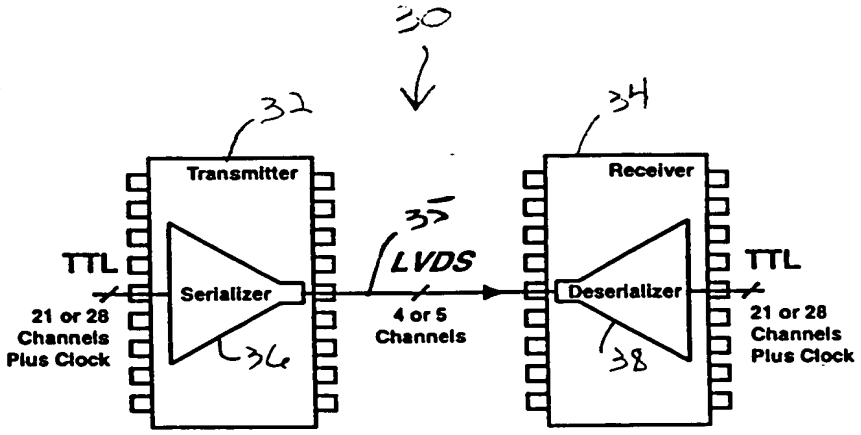

Fig. 2
(Prior Art)

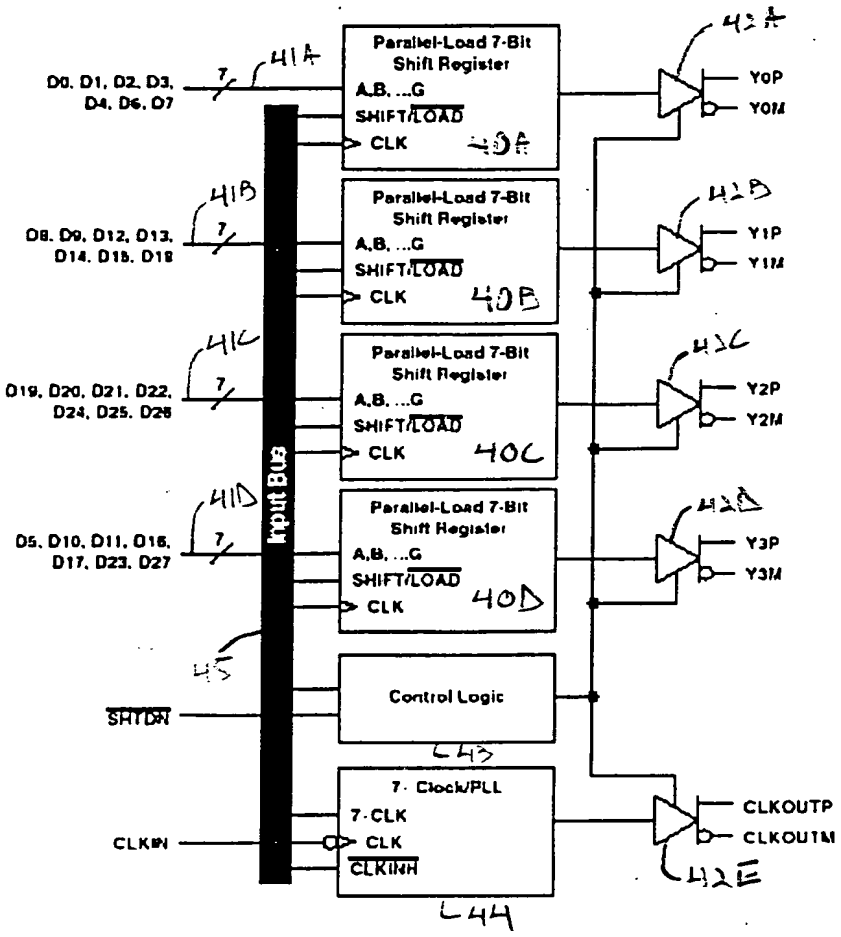

Fig. 3
(PRIOR ART)

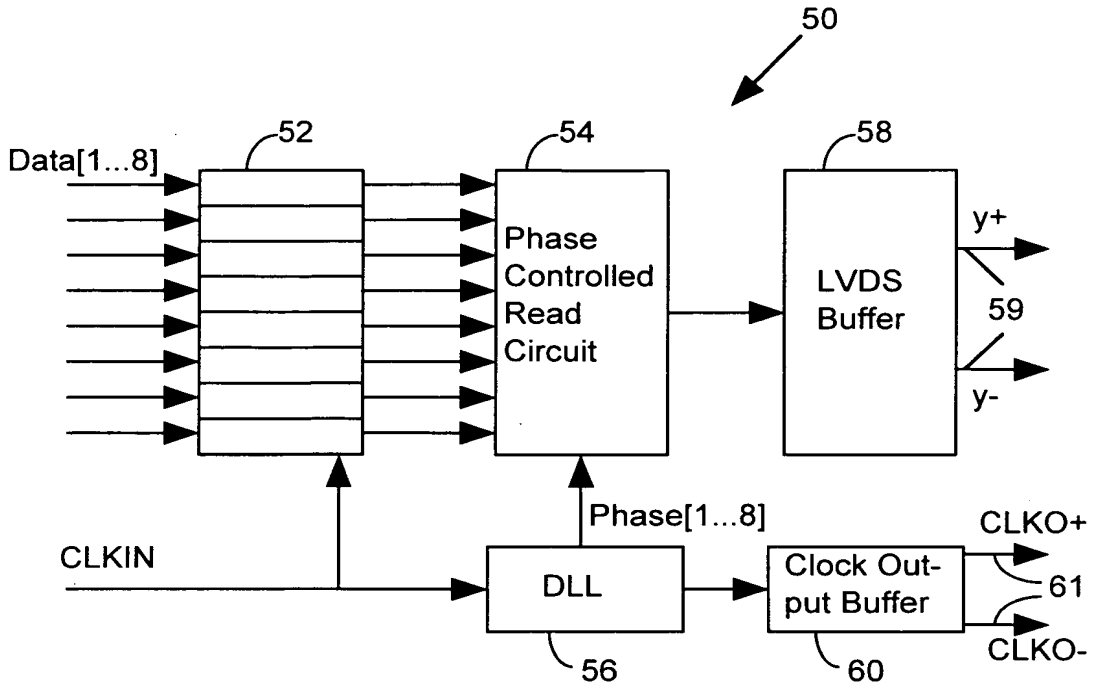
50
52
54
58
Data[1...8]
Phase
Controlled
Read
Circuit
LVDS
Buffer
y+
59
y-
Phase[1...8]
CLKIN
DLL
Clock Out-
put Buffer
CLKO+
61
CLKO-
56
60

Figure 4

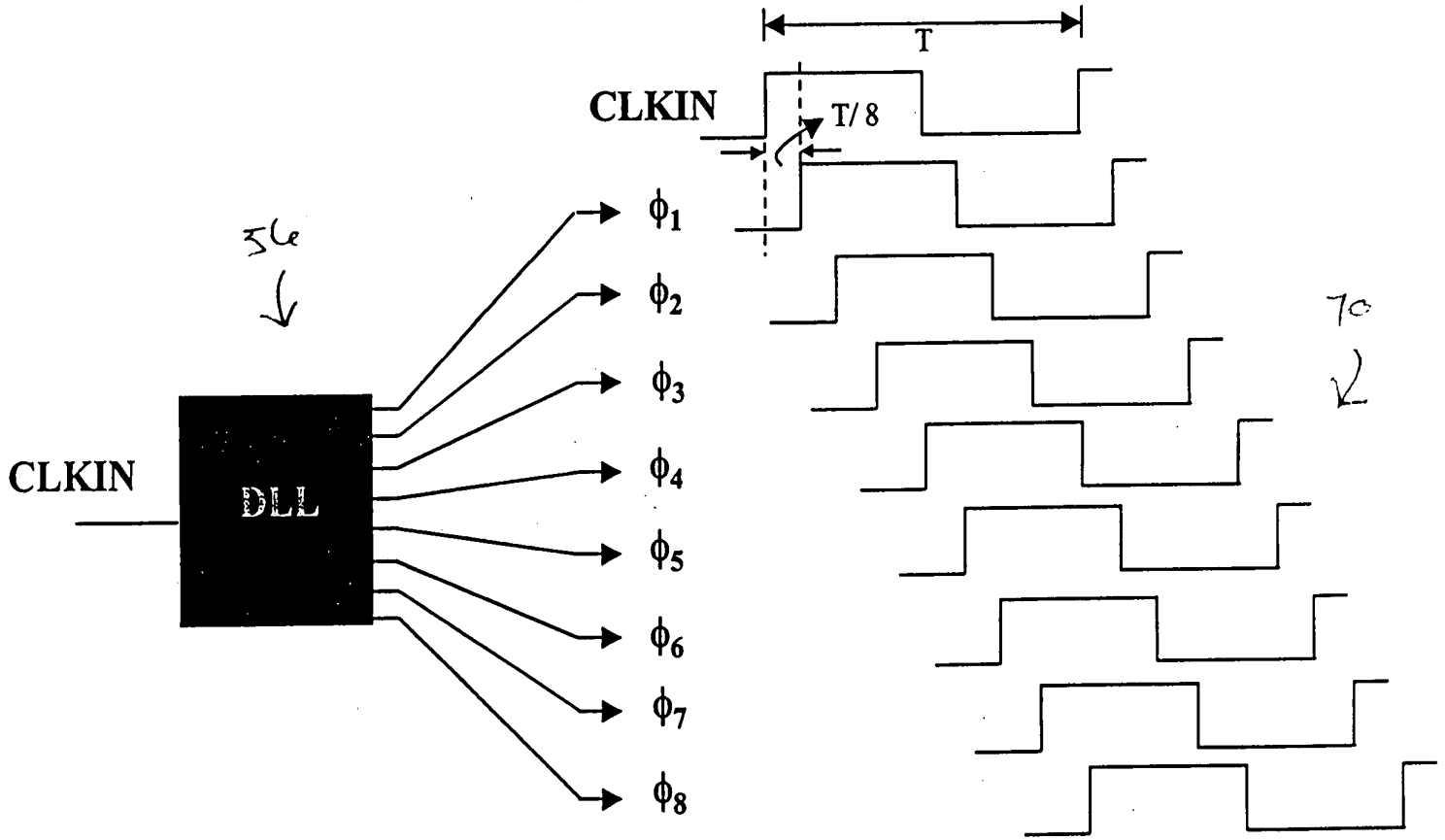

Fig. 5

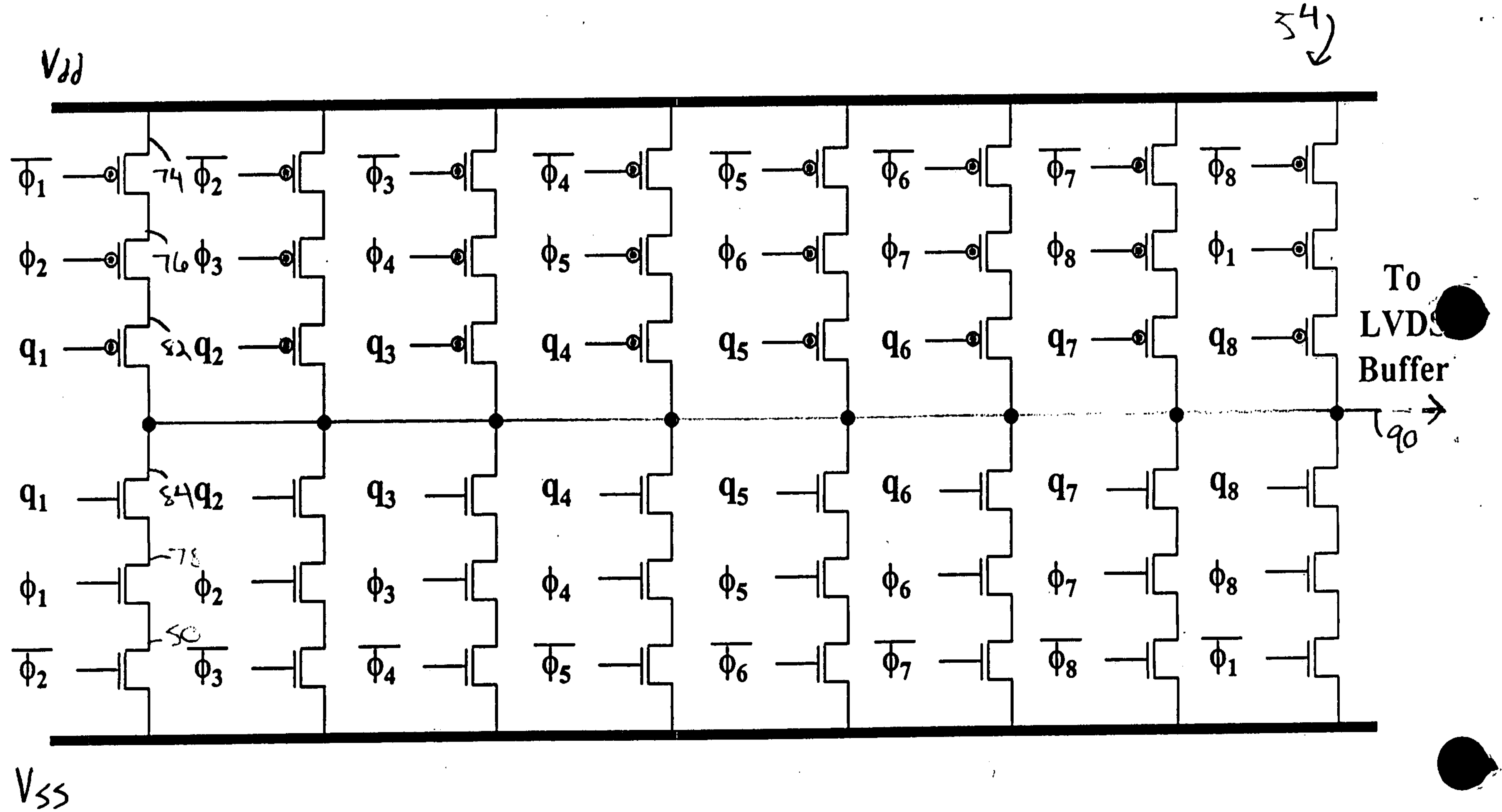

Fig. 6

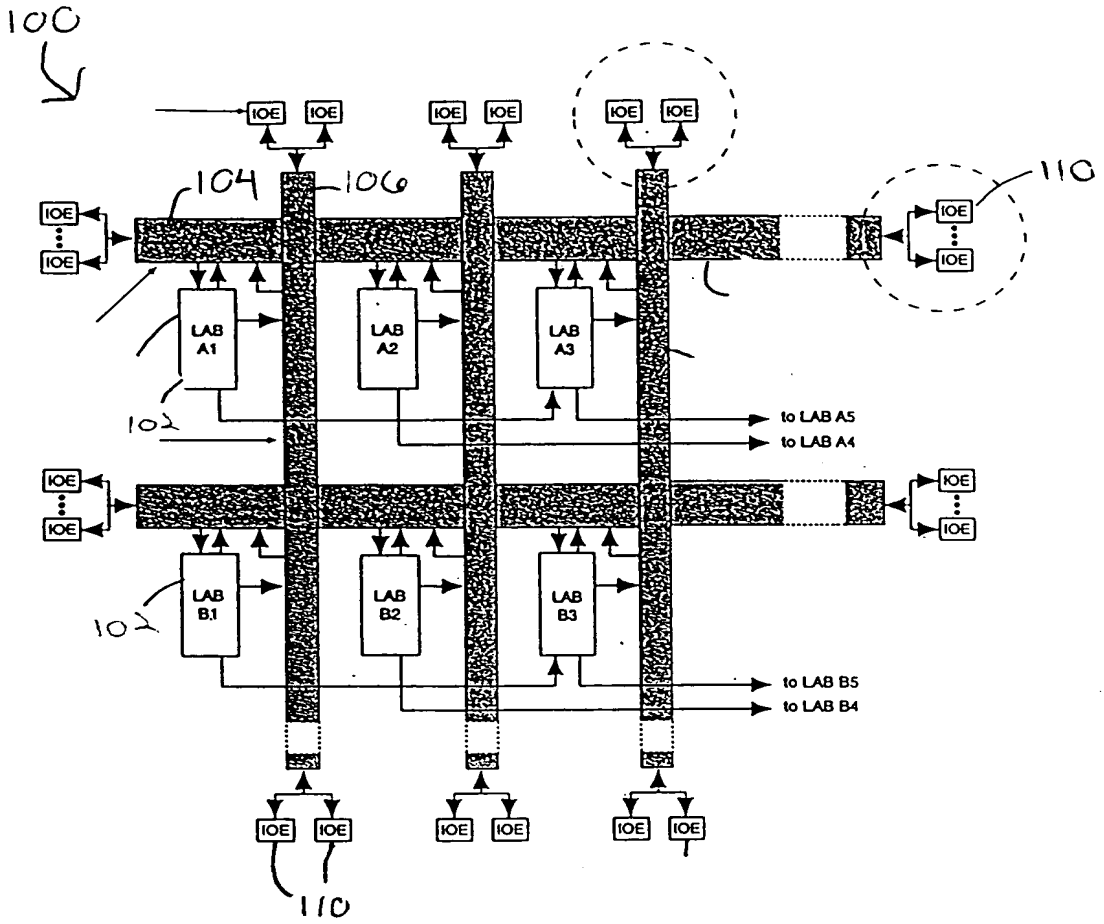
100
IOE
104
106
110
LAB A1
LAB A2
LAB A3
102
to LAB A5
to LAB A4
LAB B1
LAB B2
LAB B3
to LAB B5
to LAB B4

Fig. 7

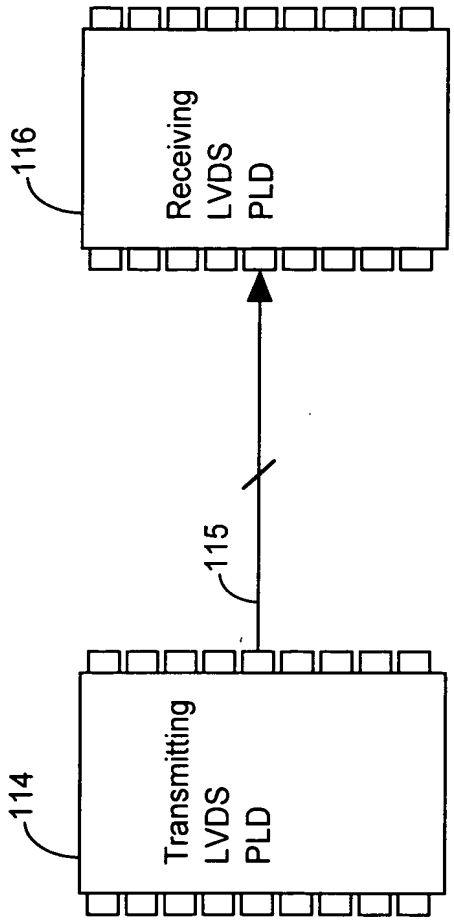

Figure 8

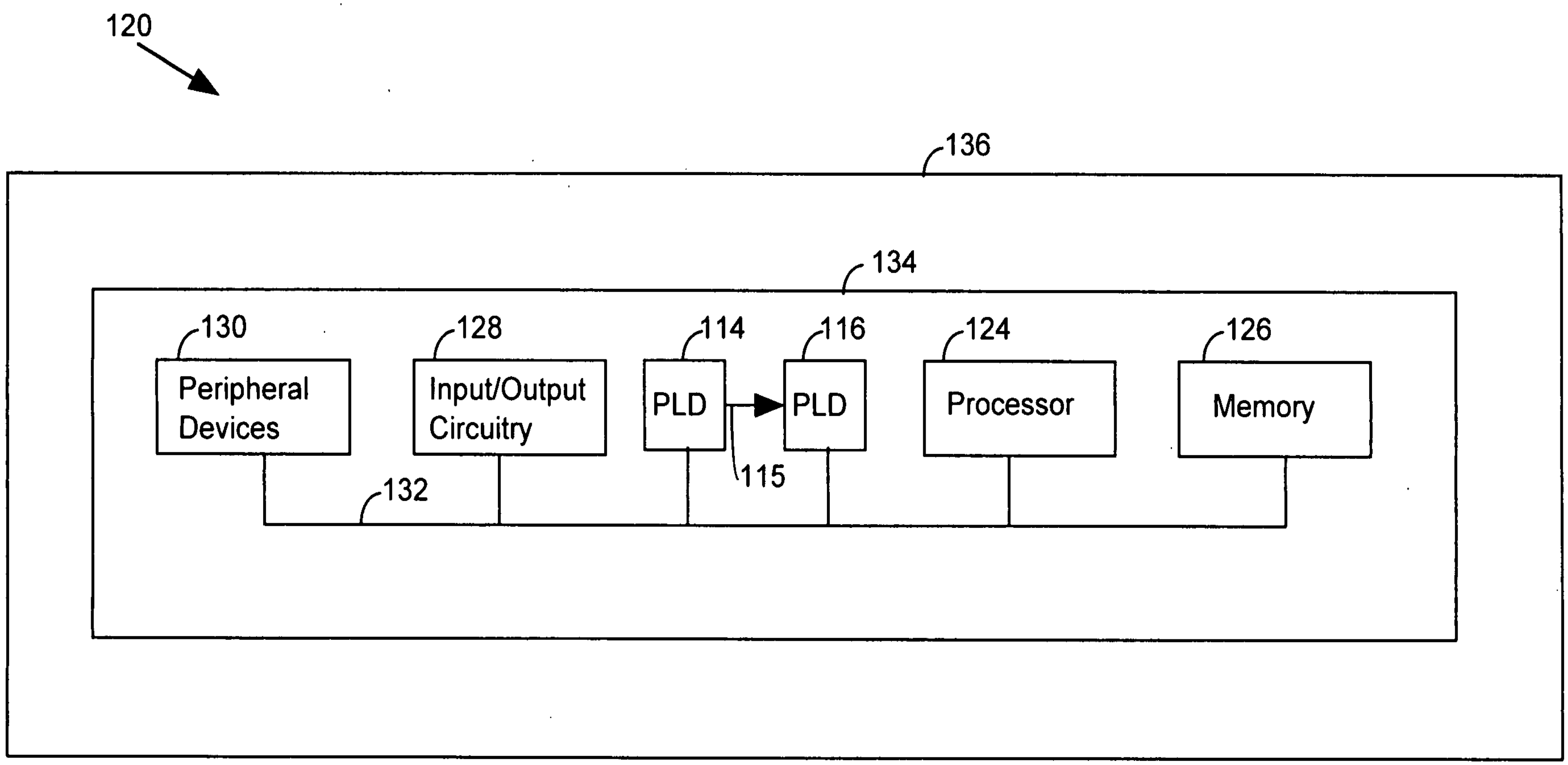
120
136
134
130
Peripheral Devices
128
Input/Output Circuitry
114
PLD
116
PLD
115
124
Processor
126
Memory
132

Figure 9

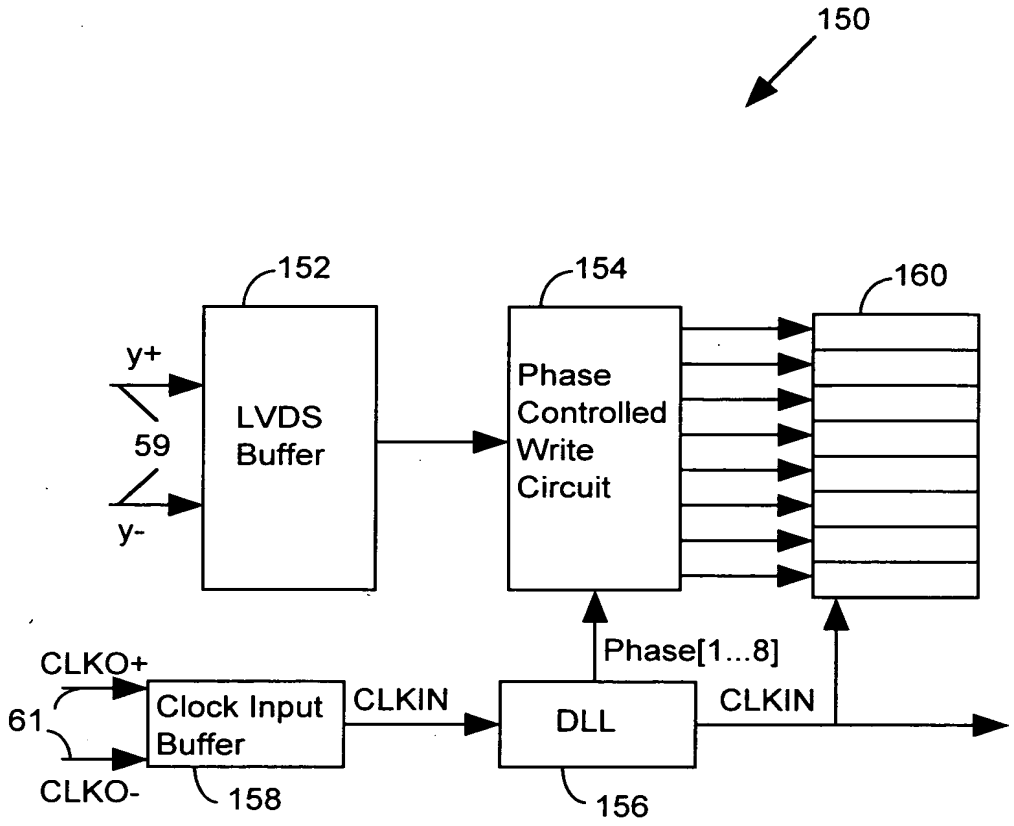
150
152
154
160
y+
59
y-
LVDS
Buffer
Phase
Controlled
Write
Circuit
CLKO+
61
CLKO-
Clock Input
Buffer
158
CLKIN
DLL
156
Phase[1...8]
CLKIN

Figure 10